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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,739	11/20/2003	Tomoki Ono	245402008000	3121

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EXAMINER	
RAO, SHRINIVAS H	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/719,739	ONO ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/20/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of paper submitted under 35 U.S.C. 119(a)-(d), claiming priority from Japanese Patent Application Nos. 2002-336660 and 2003-376,144 which papers have been placed of record in the file.

Information Disclosure Statement

Acknowledgment is made of receipt of Applicant's Information Disclosure Statement (PTO-1449) filled .

The references on PTO 1499 submitted on 11/20/2003 are acknowledged. All the cited references have been considered.

However the foreign patents and documents cited by applicant are considered to the extent that could be understood from the abstract and drawings.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (U.S. Patent No. 6,121,634, herein after Saito).

(Paper copies of cited U.S. patents and U.S. patent application publications will ceased to be mailed to applicants with Office Actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with Office Actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources. Applicants' are referred to the Electronic Business Center (EBC) at http://www.uspto.gov/ebc/index.html or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted).

With respect to claim 1 Saito describes nitride semiconductor light emitting device comprising at least a substrate, (Saito fig. 6A # 200 , col. 8 line 19) an active layer formed of a nitride semiconductor containing mainly In and Ga, (Saito fig. 6A #205, col. 8 line 24-25) a p-electrode, (Saito fig. 6A #211, col. 8 lines 32-33) and an n-electrode, (Saito figure 6A # 210, col.8 line 32) wherein at least one of said p-electrode and said n-electrode is electrically separated into at least two regions. (Saito figure 6A 211 and 210 are separated at least by two regions).

With respect to claim 2 Saito describes the nitride semiconductor light emitting diode according to claim 1, wherein at least one of said p-electrode and said n-electrode is electrically separated into at least two regions, (Saito figure 6A #s 211 and 210 are

separated at least by two regions) and said nitride semiconductor light emitting device has self pulsation characteristics. (Saito Abstract lines 4-6) .

With respect to claim 3 Saito describes the nitride semiconductor light emitting device according to claim 1, wherein said active layer has a bandgap of at least 2.6 eV, (Siato col. 7 line 8 operation voltage 3.8 V) and at least one of said p-electrode and said n-eledrode is electrically separated into at least two regions, (Saito figure 6A #s 211 and 210 are separated at least by two regions) and said nitride semiconductor light emitting device has self pulsation characteristics. (Saito Abstract lines 4-6) .

With respect to claim 4 Saito describes the nitride semiconductor light emitting device according to claim 1, wherein said active layer has a bandgap of at least 2.6 eV, (Siato col. 7 line 8 operation voltage 3.8 V) and at least one of said p-electrode and said n-electrode is electrically separated into at least two regions, (Saito figure 6A #s 211 and 210 are separated at least by two regions) and said nitride semiconductor light emitting device has self pulsation characteristics in a light output range of at least 5 mW. (Saito col. 7 lines 14-16).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (U.S. Patent No. 6,121,634, herein after Saito), as applied to claims 1-4

above and further in view of Yoshida et al. (U.S. Patent No. 5,663,975, herein after Yoshida) .

With respect to claim 5 Saito describes the nitride semiconductor light emitting diode according to claim 1, wherein at least one of said p-electrode and said n-electrode is electrically separated into at least two regions, (Saito figure 6A #s 211 and 210 are separated at least by two regions).

Saito does not specifically describe the p-electrode and n-electrode are electrically short-circuited in at least one of the regions of said separated electrode.

However, Yosihda, patent from the same filed of endeavor, describes in figure 9 and col. 11 lines 19-25 describes the p-electrode (drive region first laser resonator) and n-electrode (drive region fourth laser resonator or vice versa) are electrically short-circuited in at least one of the regions of said separated electrode, to provide a common drive region and a total of operating currents supplied to the respective drive regions and the common drive region is made constant , whereby a temperature of the laser chip can be retained always substantially constant.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include Yoshida's element of the p-electrode (drive region first laser resonator) and n-electrode (drive region fourth laser resonator or vice versa) are electrically short-circuited in at least one of the regions of said separated electrode in Saito's device . The motivation to make the above mentioned inclusion is to provide a common drive region and a total of operating currents supplied to the respective drive

regions and the common drive region is made constant, whereby a temperature of the laser chip can be retained always substantially constant. (Yoshida col. 11 lines 19-32).

With respect to claim 6 Saito describes the nitride semiconductor light emitting device according to claim 1, wherein at least one of said p-electrode and said n-electrode is electrically separated into at least two regions,(Yoshida fig.9 , regions 318 a to d) and the p-electrode and n-electrode are electrically short-circuited in at least one of the regions of said separated electrode, (Yoshida figure 9 and col. 11 lines 19-25) and said nitride semiconductor light emitting device has self pulsation characteristics. (Saito Abstract lines 4-6) .

With respect to claim 7 Saito describes the nitride semiconductor light emitting device according to claim 1, wherein said active layer has a bandgap of at least 2.6 eV, (Siato col. 7 line 8 operation voltage 3.8 V) and at least one of said p-electrode and said n-electrode is electrically separated In to at least two regions,(Yoshida fig.9 , regions 318 a to d) and the p-electrode and n-electrode are electrically short-circuited in at least one of the regions of said separated electrode, (Yoshida col. 11 lines 19-25) and said nitride semiconductor light emitting device has self pulsation characteristics. (Saito Abstract lines 4-6).

With respect to claim 8, Saito describes the nitride semiconductor light emitting device according to claim 1, wherein said active layer has a bandgap of at least 2.6 eV, (Siato col. 7 line 8 operation voltage 3.8 V) and at least one of said p-electrode and said n-electrode is separated electricity into at least two regions, ,(Yoshida fig.9 , regions 318 a to d) and the p-electrode and n-electrode are electrically short-circuited in at least

one of the regions of said separated electrode, and said nitride semiconductor light emitting device has self pulsation characteristics in a light output range of at least 5 mW. (Saito col. 7 lines 14-16).

With respect to claim 9, Saito describes the nitride semiconductor light emitting device according to claim 1, wherein one of said electrodes electrically separated into at least two regions forms contact with one of two mirror facets forming a cavity, (Yoshida figures 9 ,16-22, col. 12 lines 3 to 6, col. 18 lines 7-10) and said mirror facet has a reflection film containing a conductive material, (Yoshida figures 9 ,16-22, col. 12 lines 3 to 6, col. 18 lines 10-16) and the p-electrode and n-electrode are electrically connected by said reflection film. (Yoshida figure 9, col. 12 lines 7-15).

With respect to claim 10 Saito describes the nitride semiconductor light emitting device according to claim 9, wherein one of said electrodes electrically separated into at least two regions forms contact with one of two mirror facets forming a cavity at a side opposite to an output plane. (Yoshida figures9, 16 , etc.).

With respect to claim 11, Saito describes the nitride semiconductor light emitting device according to claim 9, wherein said conductive material includes Al.(Yoshida col.11 line 57).

With respect to claim 12, Saito describes the nitride semiconductor light emitting device according to claim 1, wherein a resistor is provided between said p-electrode and said n-electrode in at least one of the regions of said electrode electrically separated into at least two regions. (Yoshida claim 14)

With respect to claim 13, Saito describes the nitride semiconductor light emitting device according to claim 2, wherein self pulsation characteristics are adjusted by said resistor provided between said p-electrode and said n-electrode. (Yoshida claim 14)

With respect to claims 14 and 15 , Saito describes the nitride semiconductor light emitting device according to claim 1, wherein Si is added as n type impurities into said active layer, and a concentration of said Si is 1 x 1017/cm3 to 5 % 1018/cm3. (Saito col. 6 lines 45-50, conc. Figure 2- Si as ntype impurities inherent).

With respect to claim 16, Saito describes t'he nitride semiconductor light emitting device according to claim 1, wherein at least one of said p-electrode and said n-electrode is electricity separated into at least two regions, and the p-electrode and n-electrode are electrically short-circuited in at least one of the regions of said separated electrode, and a range of 0.02 ; L1/E2 S 0.30 is established, where L1 is a total length of the region where the p-electrode and n-electrode are electrically short-circuited, and L2 is a total length of the region not short-circuited, among the electrode separate; into regions. (Yoshida figures 9, 16 , etc. and col. 18 lines 9-10).

With respect to claims 17 and 18, Saito describes the nitride semiconductor light emitting device according to claim 1, wherein connection is established such that at least one of said electrodes separated into at least two regions has reverse bias applied to said active layer and another of said electrodes separated into at least two regions has forward bias applied to the active layer. (Yoshida description of figures 9, 16 ,e tc.)

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Steven H Rao whose telephone number is (571) 272-1718. The examiner can normally be reached on Monday- Friday from approximately 7:00 a.m. to 5:30 p.m.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. The Group facsimile number is (703) 308-7724.

Steven H. Rao

Patent Examiner

October 27, 2004.

LONG PHAM
PRIMARY EXAMINER